Kezhi Li

Email: kzli24@cse.cuhk.edu.hk | kzli02@qq.com
Website: https://littleblackcq.github.io

EDUCATION

The Chinese University of Hong Kong, Computer Science and Engineering, *PhD* 2024 - Present
Shanghai Jiao Tong University, Electrical and Computer Engineering, *B.S.* 2020 - 2024

- **GPA**: 3.8/4.0

PROJECTS & PUBLICATIONS

Arisca: Open-Source Arithmetic Circuit Verification via SCA 2026

- SCA based on polynomial back-rewriting is the SOTA method for verifying arithmetic circuits like multipliers; however, the community lacks open-source tools, limiting industrial adoption.
- Developed an open-source SCA verification suite in Rust, optimizing various heuristics to achieve new SOTA performance.
- Paper (to be submitted): "Arisca: An Open-Source Tool for Arithmetic Circuit Verification Using Symbolic Computer Algebra".

Multi-Agent Agile Hardware Development via C Reference Models 2025

- While LLMs enable automated hardware code generation, current methods struggle with correctness and scalability for industrial requirements.
- Designed a multi-LLM agent workflow by Langchain inspired by industrial C-reference models to synthesize Verilog from software code. The generated RTL passes formal verification and significantly outperforms traditional models in scale.
- Paper (to be submitted): "FormalRTL: Verified RTL Synthesis at Scale".

Functional Subgraph Matching via Graph Neural Networks 2025

- Subgraph matching research is often limited to structural isomorphism; in circuit optimization, identifying functional equivalence is more challenging and critical.
- Trained a GNN to determine if a subgraph can be functionally transformed into a structural subgraph of another graph, achieving SOTA performance among GNN models.
- Published in NeurIPS 2026: "Functional Matching of Logic Subgraphs ...".

HONORS & AWARDS

CUHK PhD Fellowship 2024
Outstanding Graduate of Shanghai 2024
National Scholarship 2023
SJTU Wu Jiong & Sun Jie Excellence Scholarship (Full Scholarship) 2023

SKILLS

Languages: Python, Rust, C++, Verilog, Matlab
Frameworks & Tools: Langchain, Git Workflow
English: TOFEL Mybest 110 (Writing 28, Reading 29, Listening 30, Speaking 23)

RESEARCH INTERESTS

General: Artificial Intelligence, Electronic Design Automation (EDA), IC Optimization and Verification
Specifics: Hardware Formal Verification, Model Checking, Learning-based EDA Flow Optimization